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TECHNICAL NOTE

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SIMPLIFIED TRANSISTOR DESIGN PROCEDURES

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(11) TECHNICAL NOTE

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(6) SIMPLIFIED TRANSISTOR DESIGN PROCEDURES

by

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(11) Report ELECTROMAGNETIC RADIATION

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4.1.C.

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PREFACE

Transistor design procedures, found useful in Advanced Development Electromagnetic Radiation efforts, are presented here. ~~They are derived from various literature sources as referenced in the appendix and bibliography~~. This compilation of procedures has been selected to make use of the methods employing hybrid parameters and those generally eliminating rigor associated with the more formal methods of analysis.

Accuracy for each individual problem must ultimately be decided by the designer. In most cases, it will be found to be adequate, but where it is not, an initial step toward outlining a more detailed method will be found in the references of the bibliography.

These procedures include bias circuit design, input impedance calculations for the common emitter, voltage gains calculations for the common emitter, input-output impedance of the emitter-follower stage, and power output of class A and B Amplifiers. Consideration is given to tuned harmonic multiplier efficiency.

1. USE OF THE HYBRID PARAMETERS (Reference 1)

In the application of vacuum tubes or other active devices, such as, magnetic amplifiers, the device transfer characteristics are a first necessity. The values of

$$r_p = \frac{dE_p}{dI_p} \qquad u = \frac{dE_p}{dE_c} \qquad gm = \frac{dI_p}{dE_c}$$

for vacuum tubes are obtained directly from the curves of the active devices themselves. All subsequent calculations (gain, etc.) will be based on these values. Similarly for transistors, the following basic formula is defined. Additionally and more complete notation will be found in the appendix.

$$h_{ie} = \frac{dV_{CE}}{dI_B} \quad V_{CE} = K \qquad h_{oe} = \frac{dI_C}{dV_{CE}} \quad I_B = K$$

$$h_{fe} = \frac{dI_C}{dI_B} \quad V_{CE} = K \qquad \mu_{re} = \frac{dV_{BE}}{dV_{CE}} \quad I_B = K$$

Proceeding with the previously obtained parameters, the following equations can be expressed for the common emitter configuration shown below:

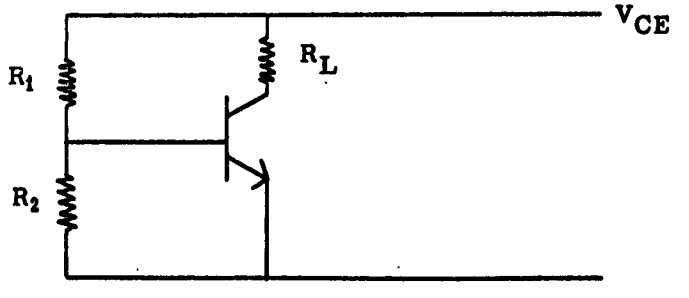
$$A_V = \frac{-h_{fe}\ R_L}{(h_{ie}\ h_{oe} - h_{fe}\ \mu_{re})\ R_L + h_{ie}} \qquad \text{VOLTAGE GAIN}$$

$$A_I = \frac{-h_{fe}}{h_{oe}\ R_L + 1} \qquad \text{CURRENT GAIN}$$

$$r_o = \frac{h_{ie} + R_G}{h_{oe}\ h_{ie} - \mu_{re}\ h_{fe} + h_{oe}\ R_G} \qquad \text{OUTPUT RESISTANCE}$$

$$r_i = \frac{h_{ie} + (h_{oc}\ h_{ie} - h_{fe}\ \mu_{re})\ R_L}{1 + h_{oe}\ R_L} \qquad \text{INPUT RESISTANCE}$$

$$A_p = \frac{(h_{fe})^2\ R_L}{(h_{oe}\ R_L + 1)\ ([h_{ie}\ h_{oe} - h_{fe}\ \mu_{re}]\ R_L + h_{ie})} \qquad \text{POWER GAIN}$$



The common collector and common base configurations may be handled with the same basic formulae provided that the subscripts denote the proper circuit employed and the hybrid parameters are measured with the proper circuit, or converted using the following expressions (Reference 12):

$$h_{ic} = h_{ie}$$
$$\mu_{re} = 1 - \mu_{re}$$
$$h_{fc} = -(1 + h_{fe})$$
$$h_{oc} = h_{oe}$$

COMMON EMITTER TO COMMON COLLECTOR

$$h_{ib} = \frac{h_{ie}}{1 + h_{fe}}$$
$$\mu_{rb} = \frac{h_{ie}\, h_{oe}}{1 + h_{fe}}$$
$$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$$
$$h_{ob} = \frac{h_{oe}}{1 + h_{fe}}$$

COMMON EMITTER TO COMMON BASE

$$h_{ie} = \frac{h_{ib}}{1 + h_{fb}}$$
$$\mu_{re} = \frac{h_{io}\, h_{ob}}{1 + h_{fc}} - \mu_{rb}$$
$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$$
$$h_{oe} = \frac{h_{ob}}{1 + h_{fb}}$$

COMMON BASE TO COMMON EMITTER

The dependency of the previous calculations consisting of the values obtained from the device, static curves, or measurements, e.g.:

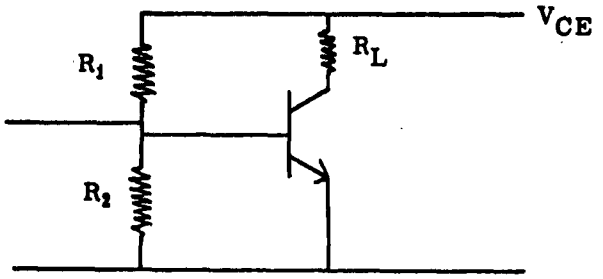
$$h_{ie} = \frac{d\, V_{BE}}{d\, I_B} \quad \text{etc.}$$

dictates that a graphical analysis of the circuit and its parameters may likely be as exact as the foregoing more formal calculations. In fact, the design will be more accurate when carried out graphically than analytically with commercial data if the graphical method were to employ the individual device curves such as are obtained from a static curve tracer. The above facts become even more impressive when the wide spread of parameters listed by the manufacturer are considered as the starting point for the calculations.

With these considerations, the designer may wish to turn his attentions to more direct, less laborious design procedures which may still provide accuracy commensurate with the use of values as listed by the device manufacturer. The following collection of design procedures is presented with this objective.

2. BIAS CIRCUIT DESIGN – NO EMITTER RESISTANCE

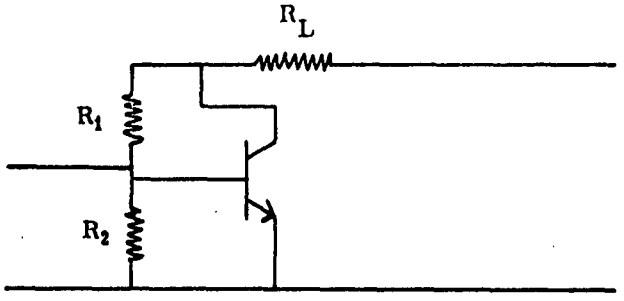
The desired operating point I_C, having been established from the graphically constructed load line, as shown on Page 8, may be provided with the following circuit:



where $I_C \cong h_{fe}\left[\frac{V_{CE}}{R_1} + I_{BCO}\right]$

neglecting R_2 and input diode voltage drop

If negative feedback is required, then the following circuit is valid.



where $I_C \cong \frac{h_{fe}\left[V_{CE} + I_{CO} R_1\right]}{R_1 + h_{fe} R_L}$

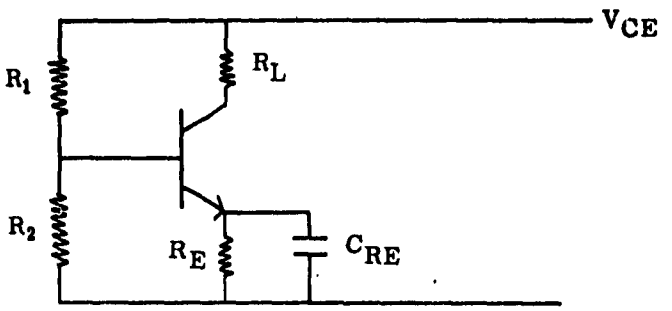
neglecting R_2 and input diode voltage drop

If R_2 is used in either of the above two cases (to stabilize the bias source), there must be an accountability for a further reduction of the bias voltage. Thus if $R_2 = R_1$, then I_C of twice the desired value must be used in the calculations.

The second method provides little temperature stabilization and the first none, therefore these procedures require the use of special biasing resistors, such as sensistors, or other devices.

3. BIAS DESIGN FOR THE COMMON EMITTER CONFIGURATION (Reference 2)

The most commonly used bias arrangement, as shown below, provides an emitter resistance for temperature stabilization (Reference 16). Stabilization of h_{fe} and other parameters is discussed in Reference 19.



R_E normally ranges from 500 to 1000 ohms for small devices and is bypassed by C_{RE} for the lowest desired signal frequency. R_2 is best limited in value from 5 to 10 times R_E to provide a rigid bias point. R_1 is used to divide the collector supply voltage with R_2 in order to provide the desired operating bias current

$$I_B \cong \frac{V_{BE}}{R_E} \qquad \text{(neglecting input diode voltage drop)}$$

as determined from the load line or other means. The desired operating point in terms of collector current may be obtained likewise

$$I_C \cong \frac{V_{CE}\, R_2}{R_E (R_1+R_2)} .$$

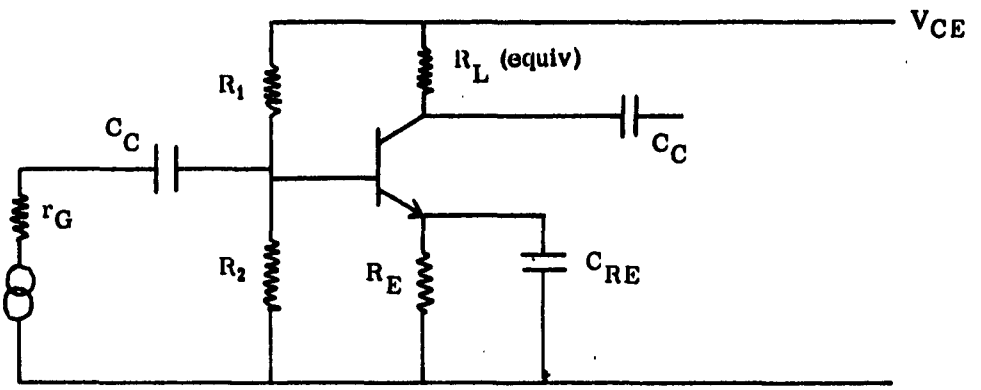
A more rigorous method for bias control of I_{CBO} drift may be found in Reference 2.

4. INPUT IMPEDANCE CALCULATIONS FOR THE COMMON EMITTER (Reference 3)

To determine the "circuit" input resistance of a common emitter stage shown on Page 5, the following expression may be used:

$$R_{in} = \left[1 + h_{fe}\right] h_{ib} \quad \left(\text{neglecting } \frac{R_1 R_2}{R_1 + R_2} \text{ effect}\right)$$

Typically this value ranges from 1000 to 3000 ohms and increases principally with increasing values of h_{fe}.



5. VOLTAGE GAIN CALCULATIONS FOR THE COMMON EMITTER (Reference 3)

The AC voltage gain at 1 KC from the common emitter amplifier shown above is approximately equal to

$$A_v \cong \frac{-R_L}{h_{ib}} \cong \frac{e_{OUT}}{e_{IN}}$$

with h_{ib} as normally specified in the manufacturer's data sheets.

The value of R_L must reflect the effects of any subsequent stage loading, e.g.:

$$R_L = \frac{R_{IN}\, R_c}{R_{IN} + R_c}$$

where R_c = collector load resistor, and

R_{IN} = next stage input resistance.

The AC voltage gain ≅ -3 DB of the 1 KC value at a frequency:

$$f\ (-3DB) \cong \frac{1 + h_{fe}}{2\pi\, C_C\, r_G}$$

where C_C = coupling capacity, and

r_G = generator resistance.

6. VOLTAGE GAIN OF TWO SIMILAR R-C COUPLED COMMON EMITTER (Reference 4)

The voltage gain of two stages as shown on Page 5 and connected in cascade is

$A_v \cong h_{fe} \frac{R_L}{h_{ib}}$ with the second stage input resistance becoming the first stage load resistance. The expression for the voltage gain of the two stages is therefore much smaller than the product of the separate gains, e.g.:

$$A_v \cong h_{fe} \frac{R_L}{h_{ib}} << \left(\frac{R_L}{h_{ib}} \right)^2$$

This loss may almost completely be recovered with the use of an emitter-follower stage between the common emitter stages, to transform the medium high output impedance to a lower input impedance, with small losses (.9 typically).

7. INPUT-OUTPUT IMPEDANCE OF THE EMITTER FOLLOWER STAGE (Reference 5 and 20)

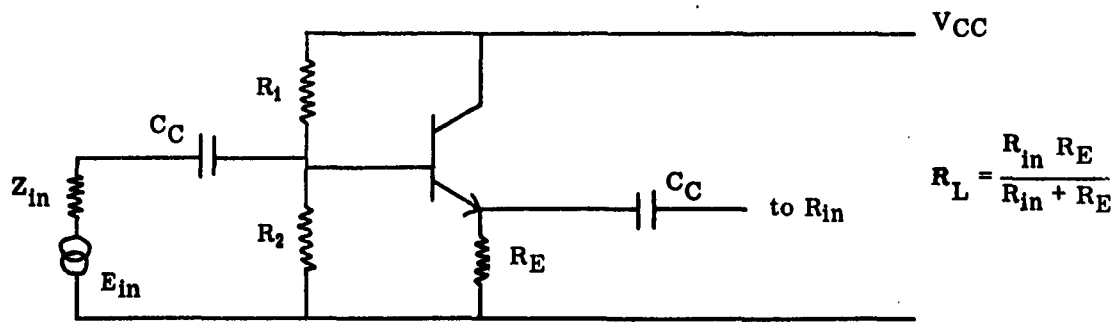
The output impedance Z_o for the emitter follower (common collector) connection as shown below is equal to approximately

$$\frac{Z_{eq}}{h_{fe}} \cong Z_o$$

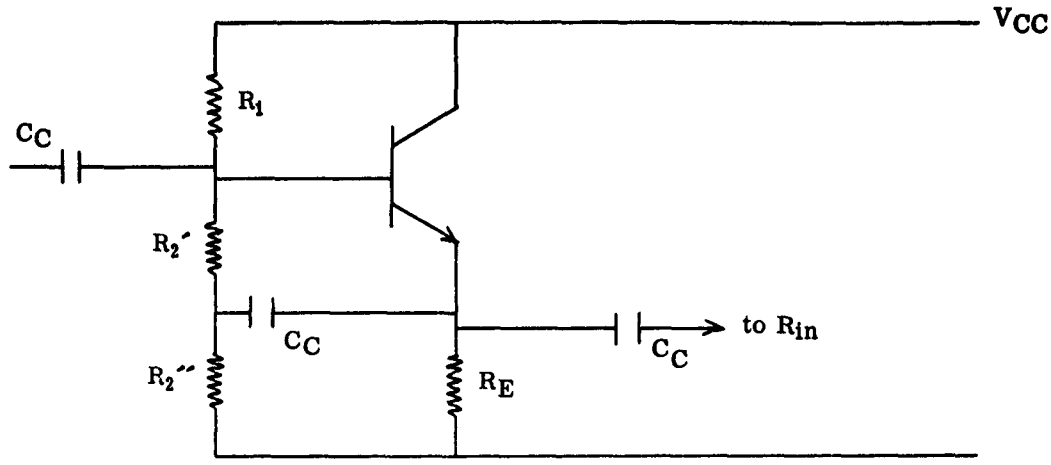
where Z_{eq} is the resultant of R_1, R_2 and Z_{in}.

The input impedance is equal to

$$h_{fe} R_L \cong Z_{in}$$



The imput impedance may be further increased by bootstrapping the bias return to the signal output as shown below and described in Reference 22.



$R_2 = R_2' + R_2''$ (conditional with stability factors)

8. POWER OUTPUT OF CLASS A AND B AMPLIFIERS (Reference 6)

The maximum power output obtainable from a Class A amplifier, as shown with a central operating point below and without clipping, is equal to

$$P_o = \frac{E_C I_C}{2}$$

The necessary load resistance

$$R_L = \frac{E_c}{I_C} = \frac{E_c^2}{2 P_o}$$

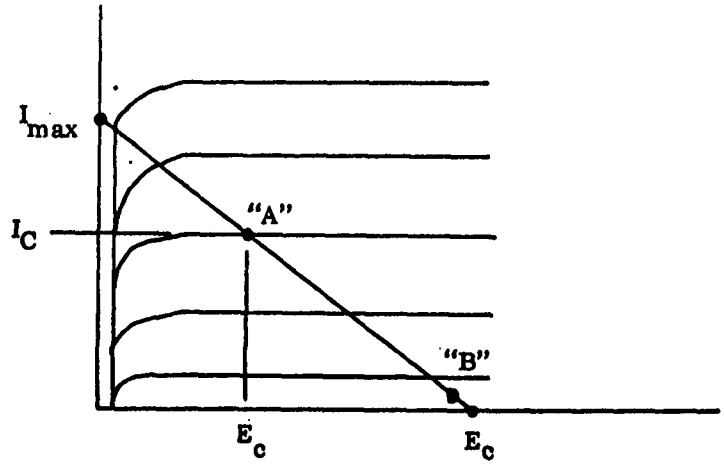
The maximum power output obtainable from a Class B amplifier, shown below with a near cutoff operating point and without clipping, is equal to

$$P_o = \frac{I_{max} E_c}{2}$$

The necessary load resistance

$$R_L = \frac{E_c}{I_{max}} \qquad \text{(LOAD LINE)}$$

$$R_{cc} = \frac{2 E_c^2}{P_o} \qquad \text{(COLLECTOR TO COLLECTOR)}$$



9. TUNED HARMONIC MULTIPLIER EFFICIENCY (Reference 21)

The approximate output power that may be obtained with the tuned (high Q RF circuits) harmonic multiplier is given by

$$P_{OUT} \cong \left(\frac{1}{n}\right)^2 P_o$$

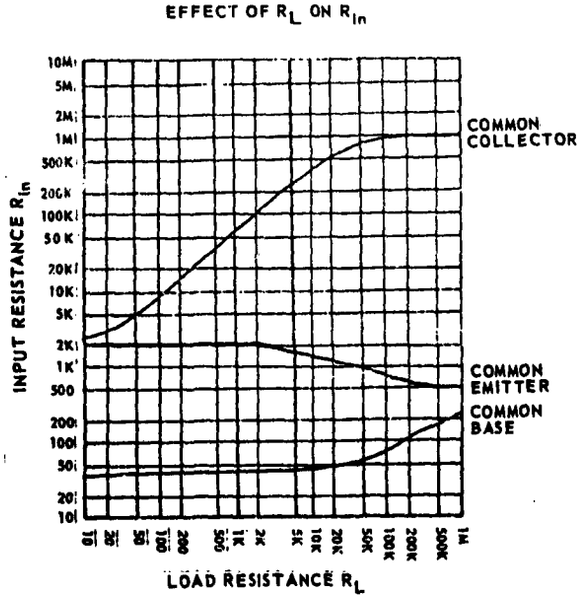
where P_o = Class "C" RF output, and

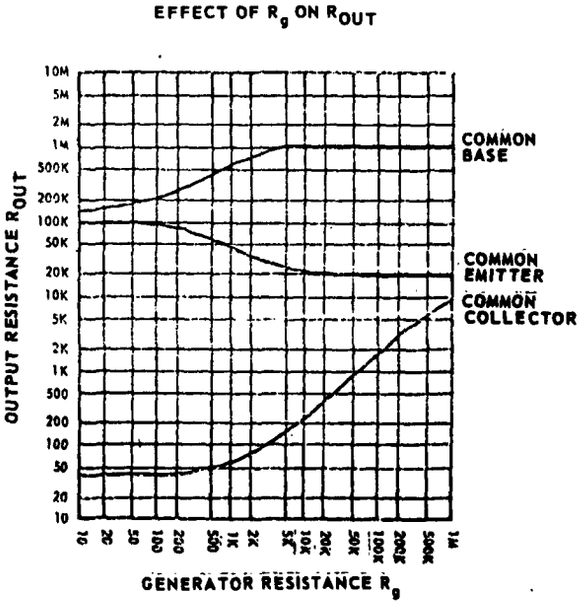
n = harmonic being amplified.

Optimum harmonic output power, as calculated above, is directly dependent upon the operating bias, and the emitter resistance must be empirically determined for each harmonic sought.

10. EFFECTS OF LOAD AND GENERATOR RESISTANCE FOR EACH CONFIGURATION (Reference 7)

Application of any of the preceding procedures will be greatly enhanced with knowledge of the magnitude and direction of the reflected parameters. These effects have been presented here in the following curves.





APPENDIX

Hybrid parameters are a mixture of Z and Y parameters, impedance and conductance, etc. obtained with the aid of general network equations as written for four terminal networks. Other simplified design techniques are available, notably using "r" parameters, and are derived with the equivalent "T" circuit (Reference 17). These techniques depend upon the use of empirical or measured data, and are not generally listed by the device manufacturer because they are inconvenient to manipulate.

The following often used h parameter notation is presented here with subscripts denoting the most commonly measured configuration, e.g., h_{fe} = Current Gain Common Emitter. The same type notation may apply to any configuration with the use of appropriate subscripts, e.g., h_{ib} = Input Impedance Common Base. Upper case subscripts generally denote DC values and lower case subscripts generally denote AC values.

A. SUPPLY PARAMETERS – USUALLY MAXIMUMS (Reference 8)

Collector supply voltage	V_{CE}
Base supply voltage	V_{BE}
Collector current	I_C
Base current	I_B
Junction temperature	T_J

B. DEVICE PARAMETERS – DC

Forward current gain (V_{ce} specified)	h_{FE}
Collector cutoff current	I_{CBO}
Emitter cutoff current	I_{EBO}
Collector to emitter breakover voltage	BV_{CES}

C. DEVICE PARAMETERS – AC SMALL SIGNAL

Forward current gain "β" or "α_{fe}" (output AC shorted)	h_{fe}
Input impedance (output AC shorted)	h_{ib}
Output admittance (input AC open)	h_{ob}
Output capacity (input open; frequency specified)	C_{oe}

Cutoff frequency (Frequency where gain = .707 h_{fe})	f_{ac}
Noise figure	NF
Collector saturation voltage (offset voltage; I_C specified)	$V_{CE\ (SAT)}$
Collector saturation resistance (I_C and I_B specified)	R_{CS}

D. DEVICE PARAMETER DEFINITIONS – DC (Reference 9)

$$H_{FE} = \frac{I_C}{I_B} \qquad G_M = \frac{I_C}{V_{BE}}$$

$$H_{IE} = \frac{V_{BE}}{I_B} \qquad R_S = \frac{V_{CE}}{I_C}$$

NOTE: These definitions contain upper case letters, e.g., H_{FE} to denote "DC" hybrid measurements (Reference 10).

E. CIRCUIT MATRIX NOTATION (Reference 11)

The circuit notations shown below, and their equals in terms of hybrid parameters, are less often used in transistor analysis alone, but are generally used to solve any four terminal network problems. They are mainly used with an additional subscript to denote the circuit employed (Reference 14) e.g.,

$h_{11} = h_i = h_{ic}$

$h_{11} = h_i$ = input impedance (output AC shorted)

$h_{22} = h_o$ = output conductance (input AC open)

$h_{21} = h_f = \beta$ or forward AC current gain (output AC shorted)

$h_{12} = h_{rc}$ = reverse resistance (input open)

F. TYPICAL VALUES OF THE IMPORTANT h PARAMETERS (References 13 and 15)

Parameter	h_{ib} Ω	h_{ie} Ω	h_{fc}	h_{ob} umho	h_{oc} umho
WE 2N463		28-51	50-91		
RCA 2N301		23	75		
Minn. Honeywell 2N540		24-60	50-150		
Texas Inst. 2N1047		500	12-90		
Bendix 2N1008		200-1000	40-150		300
Texas Inst. 2N336	30-80		76-333	.25	
Texas Inst. 2N1382	30		80	.5	

Occasionally it may be desirable to employ r parameters in design, which may be converted as follows:

$$r_e = h_{11} - \frac{h_{12}}{h_{22}} (1 + h_{21}) = h_i - \frac{h_{rc}}{h_o} (1 + h_f)$$

$$r_b = \frac{h_{12}}{h_{22}} = \frac{h_{rc}}{h_o}$$

$$r_c = \frac{1}{h_{22}} = \frac{1}{h_o}$$

$$\beta = \frac{h_{21}}{1} = -h_f$$

BIBLIOGRAPHY

Reference Number	
1	U.S. Army Technical Manual 11-690 p. 77 (α_{fe} is used here in place of β)
2	Third Edition G.E. Transistor Manual p. 15.
3	Third Edition G.E. Transistor Manual p. 18
4	Third Edition G.E. Transistor Manual p. 19
5	Electrical Industries Magazine
6	Third Edition G.E. Transistor Manual p. 20
7	U.S. Army Technical Manual 11-690 p. 109
8	This data has been abstracted from current manufacturers data sheets
9	Additional rigorous design equations and their simplifications, using both r and h parameters may be found in "Transistor Circuits and App" by Carrol p. 20-24
10	As detailed for the 2N463 by Western Electric Co.
11	This older basic method is described in detail in "Transistor circuit application course" by Sam Nissin p. 38
12	As found in U.S. Army Technical Manual 11-690 p. 79
13	This data has been abstracted from current manufacturer's data sheets.
14	Additional notations and their equivalents which have been used may be found in U.S. Army Technical Manual 11-690 p. 80
15	Recommended letter symbols to be used for semiconductor data sheets and specifications are presented in EIA Standard No. RS-245
16	An account of amplifier bias operation using the emitter resistor R_E and its effects on the bias values, may be found in "Introduction to Junction Transistors" by R.C.A. p. 13
17	A summary of practical equations using r parameters is to be found in "Transistor Circuit Design" by Texas Instrument p. 98
18	Texas Instruments application notes for April 1960
19	Texas Instruments application notes for March 1961
20	Philco application lab report 701B, p. 4
21	Philco application lab report 701B, p. 19
22	Philco application lab report 622

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